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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,716	02/09/2004	Balaji Natarajan	015114-071000US	3838
26059	7590	04/05/2005	EXAMINER	
TOWNSEND AND TOWNSEND AND CREW LLP/ 015114			NGUYEN, VINH P	
TWO EMBARCADERO CENTER			ART UNIT	
8TH FLOOR			PAPER NUMBER	
SAN FRANCISCO, CA 94111-3834			2829	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/775,716

Applicant(s)

NATARAJAN ET AL.

Examiner

VINH P. NGUYEN

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 8, 11-12, 15 is/are rejected.
- 7) ☒ Claim(s) 6, 7, 9, 10, 13, 14 and 16-25 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
2. The abstract of the disclosure is objected to because legal phraseology such as “the present invention” is used. Correction is required. See MPEP § 608.01(b).
3. The disclosure is objected to because of the following informalities: it appears that the detailed description of “a retiming circuit” is not provided. What does “a retiming circuit” comprises of.

Appropriate correction is required.

4. Claims 6-7, 9-10, 13-14 and 16-25 are objected to because of the following informalities:

In claims 6, 13, it is unclear what is meant by “retiming the test output data”.

Furthermore, it is unclear what does “retiming circuit” comprise of in order to retiming the test output data .

In claim 9, it is unclear what is meant by “the delayed test output data and test data are retimed”. Furthermore, it is unclear what does “retiming circuit” comprise of in order to retiming the test output data.

In claim 16, it is unclear how the plurality of logic elements and the interconnect lines are interrelated and associated with the delay circuit, the first compare circuit and the second compare circuit.

In claims 18-19 and 21, it is unclear what “retiming circuit” comprises of.

The dependent claims 7, 10, 14, 17, 20, 22-25 not specifically address share the same indefiniteness as they depend from objected claims

Appropriate correction is required.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-5 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Benavides (Pat # 6,618,827).

As to claim 1, Benavides disclose an apparatus as shown in figure 1 having a chain selection (100) for receiving test output data (TDO) from a circuit under test, a delay adjustment device (200) for delaying the test output data from the chain selection (100), comparator (400) for comparing the delay test data output with test data output (E) and outputting a first compare signal (F) if the test data output (E) is not the same as the delay test output signal (C) , comparison control (300) for generating a control signal (K) and a status collection (500) for

comparing the first compare signal (F) with the control signal (K) and providing a second compare signal.

As to claims 2-3, it appears that the second compared signal toggles from a first state to a second state while receiving the test output data by the shift signal (G) from the shifter (600) then provide a signal indicating an error or no error.

As to claim 4, it appears that the control signal is changed by the TCK,TMS signals therefore the test output data (E) is also toggled.

As to claim 5, it appears that when the control signal (K) is changed, the second compare signal toggles between the first stage to the second state (from indicating error to no error).

As to claim 8, it appears that the delay is done by delay adjustment device (200) using flip flop as shown in figure 3.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 12 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Mattison (Pat # 5,867,332).

As to claim 12, Mattison discloses a window margining apparatus as shown in figure 7A

having a delay circuit (114), a first compare circuit (120) connected to the delay circuit (114) and a second compare circuit (122) coupled to the first compare circuit (120) and further coupled to receive a control signal from Exclusive Or (118).

As to claim 15, the first and second compare circuits (120,122) are Exclusive OR gates.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Benavides (Pat # 6,618,827) in view of Mattison (Pat # 5,867,332).

Benavides discloses an apparatus as shown in figure 1 having a chain selection (100) for receiving test output data (TDO) from a circuit under test, a delay adjustment device (200) for delaying the test output data from the chain selection (100), comparator (400) for comparing the delay test data output with test data output (E) and outputting a first compare signal (F) if the test data output (E) is not the same as the delay test output signal (C), comparison control (300) for generating a control signal (K) and a status collection (500) for comparing the first compare signal (F) with the control signal (K) and providing a second compare signal. Benavides does not teach that the first and second compare signals are done using first and second Exclusive OR gates.

However, Mattison teaches that it would have been well known to use the first and second Exclusive Ors (120,120) for providing the first and second compare signals. It would have been well known for one of ordinary skill in the art to use Exclusive OR gates (120,122) as first and second compare circuits as taught by Mattison et al to the device of Benavides since this is an alternative types of the comparators

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Salvatore (Pat # 4,010,418) disclose transistor circuits.

Nakashimo (Pat # 6,570,426) disclose delay circuit.


Jett et al (Pat # 6,008,664) disclose parametric test system and method.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is 571-272-1964. The examiner can normally be reached on 6:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


VINH P NGUYEN
Primary Examiner
Art Unit 2829
04/01/05
